**Department of Electronics and Communication Engineering**

**DSP - Lab**

**Instructional Objectives:**

* To understand the basic function of DSP Processor, PIC, ARM, and MSP430.
* To design and implement FIR, IIR filters and Multirate signal processing in DSP processor.
* To study the various interfaces with embedded controller.
* To provide hands on design experience with professional design (EDA) platforms.
* To familiarize fusing of logical modules on FPGA.

**Students Outcomes:**

At the end of the course, the student will be able to:

* Select of the processors, controllers and interfacing devices for various applications.
* Design and Implement the FIR and IIR Filters in DSP Processor for performing filtering operation over real-time signals.
* Design and Implement Wireless network using Embedded Controller.
* Design, Simulate and Extract layouts of Digital and Analog IC blocks using EDA tools.
* Design and Implement ALU / MAC circuits FPGA.

|  |
| --- |
| **Major Equipments Available in the Lab** |
| **S. No.** | **Name of the Equipments** | **Quantity** |
| 1 | Computers with LAN connection | 30 |
| 2 | TMS320C6745 DSP Trainer Kit | 15 |
| 3 | Spartan 3 Development Board | 15 |
| 4 | PIC Microcontroller Board | 5 |
| 5 | TMS320C67X DSP Trainer Kit | 5 |
| 6 | MSP430F225 16-bit Microcontroller | 5 |
| 7 | CPLD/FPGA Development Board | 10 |
| 8 | ARM 9 Development Board | 5 |
| 9 | PSoC Microcontroller Board | 2 |
| 10 | Add on cards – Train, Elevator and PLL | Each 1 |

**Department of Electronics and Communication Engineering**

**DSP - Lab**

**List of Experiments**

**Digital Signal Processing Laboratory 5th Sem ECE**

1. MATLAB / Equivalent Software Package
2. Generation of elementary Discrete-Time sequences
3. Linear and Circular convolutions
4. Auto correlation and Cross Correlation
5. Frequency Analysis using DFT
6. Design of FIR filters (LPF/HPF/BPF/BSF) and demonstrates the filtering operation
7. Design of Butterworth and Chebyshev IIR filters (LPF/HPF/BPF/BSF) and demonstrate the filtering operations
8. DSP Processor Based Implementation
9. Study of architecture of Digital Signal Processor
10. Perform MAC operation using various addressing modes
11. Generation of various signals and random noise
12. Design and demonstration of FIR Filter for Low pass, High pass, Band pass and

Band stop filtering

1. Design and demonstration of Butter worth and Chebyshev IIR Filters for Low pass,

High pass, Band pass and Band stop filtering

1. Implement an Up-sampling and Down-sampling operation in DSP Processor

**Department of Electronics and Communication Engineering**

**DSP - Lab**

**List of Experiments**

**VLSI Design Laboratory 6th Sem ECE**

Part I: Digital System Design using HDL & FPGA

1. Design an Adder (Min 8 Bit) using HDL. Simulate it using Xilinx/Altera Software and

implement by Xilinx/Altera FPGA

1. Design a Multiplier (4 Bit Min) using HDL. Simulate it using Xilinx/Altera Software and implement by Xilinx/Altera FPGA
2. Design an ALU using HDL. Simulate it using Xilinx/Altera Software and implement by Xilinx/Altera FPGA
3. Design a Universal Shift Register using HDL. Simulate it using Xilinx/Altera Software and implement by Xilinx/Altera FPGA
4. Design Finite State Machine (Moore/Mealy) using HDL. Simulate it using Xilinx/Altera Software and implement by Xilinx/Altera FPGA
5. Design Memories using HDL. Simulate it using Xilinx/Altera Software and implement

by Xilinx/Altera FPGA

Compare pre synthesis and post synthesis simulation for experiments 1 to 6. Requirements: Xilinx ISE/Altera Quartus/ equivalent EDA Tools along with Xilinx/Altera/equivalent FPGA Boards

Part-II Digital Circuit Design

1. Design and simulate a CMOS inverter using digital flow
2. Design and simulate a CMOS Basic Gates & Flip-Flops
3. Design and simulate a 4-bit synchronous counter using a Flip-Flops

Manual/Automatic Layout Generation and Post Layout Extraction for experiments 7 to 9 Analyze the power, area and timing for experiments 7 to 9 by performing Pre Layout and Post Layout Simulations

Part-III Analog Circuit Design

1. Design and Simulate a CMOS Inverting Amplifier.
2. Design and Simulate basic Common Source, Common Gate and Common Drain

Amplifiers. Analyze the input impedance, output impedance, gain and bandwidth for experiments 10 and 11 by performing Schematic Simulations.

1. Design and simulate simple 5 transistor differential amplifier. Analyze Gain, Bandwidth and CMRR by performing Schematic Simulations

**Department of Electronics and Communication Engineering**

**DSP - Lab**

**List of Experiments**

**Electronics System Design Laboratory I 1st Sem ME AE**

1. System design using PIC, MSP430, 51 Microcontroller and 16-bit microprocessor 8086
2. Study of different interfaces (using embedded microcontroller)
3. Implementation of Adaptive filters and multistage multirate system in DSP processor
4. Simulation of QMF using simulation packages
5. Analysis of asynchronous and clocked synchronous sequential circuits
6. Built in self-test and fault diagnosis
7. Sensor design using simulation tool
8. Design and analysis of real time signal processing system – Data acquisition and signal processing

**Electronics System Design Laboratory II 2nd Sem ME AE**

1. Study of 32-bit ARM7 microcontroller RTOS and its application
2. Testing RTOS environment and system programming
3. Designing of wireless network using embedded system
4. Implementation of ARM with FPGA
5. Design and Implementation of ALU in FPGA using VHDL and Verilog
6. Modelling of Sequential digital system using Verilog and VHDL
7. Flash control programming – data flash with erase, verify and fusing
8. System design using ASIC
9. Design, Simulation and analysis of signal integrity

|  |
| --- |
| **Department of Electronics and Communication Engineering** |
| **PG / DSP & VLSI - Lab** |
| **Courses Offered** |
| **S. No.** | **ODD Semester** | **Class** | **No. of Sessions** | **EVEN Semester** | **Class** | **No. of Sessions** |
| 1 | Digital Signal Processing Laboratory | 5th Sem ECE | 4 | VLSI Design Laboratory | 2nd Sem ECE | 4 |
| 2 | Electronic System Design Laboratory I | 1st Sem ME AE | 2 | Electronic System Design Laboratory II | 2nd Sem ME AE | 2 |
| Percentage of Lab Utilization : 60%  | Percentage of Lab Utilization : 60% |